REMARKS

By the present amendment and response, claims 8, 9, 15-17, and 20-22 have been amended to overcome the Examiner's objections. Claims 8, 9, 14-17, and 19-22 are pending in the present application. Reconsideration and allowance of pending claims 8, 9, 14-17, and 19-22 in view of the following remarks are requested.

A. Rejection of Claims 8 and 17 under 35 USC §102(b)

The Examiner has rejected claims 8 and 17 under 35 USC §102(b) as being anticipated by U.S. patent number 5,314,834 to Mazure et al. ("Mazure"). For the reasons discussed below, Applicants respectfully submits that the present invention, as defined by amended independent claim 8, is patentably distinguishable over Mazure.

The present invention, as defined by amended independent claim 8, includes, among other things, a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, and where the first thickness is greater than the second thickness. As disclosed in the present application, the present invention provides a NAND-type memory cell including a tunnel oxide layer having a second thickness directly over a channel region and a first thickness in an overlap region over a portion of a source region and in an overlap region over a portion of a drain region, where the first thickness is greater than the second thickness.

As disclosed in the present application, the tunnel oxide layer is first formed over the channel region and over a portion of the source and drain regions. As disclosed in the present application, the tunnel oxide layer is then recessed such that the portion of the tunnel oxide layer situated over the channel region is thinner than the portion of the tunnel oxide layer that extends over a portion of the source and drain regions. As disclosed in the present application, by forming the tunnel oxide layer such that the tunnel oxide layer is thicker in the overlap regions and thinner over the channel region, the present invention achieves a reduced injection field and a reduced current density in the overlap regions. As a result, the present invention achieves reduced tunnel oxide degradation in the overlap regions, which advantageously improves memory cell retention and endurance.

In contrast, Mazure does not teach, disclose, or suggest a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, and where the first thickness is greater than the second thickness. Mazure specifically discloses device 11 having gate 16, gate extension 26, gate dielectrics 14 and 24, and source and drain regions 28, where gate 16 is situated over gate dielectric 14, and where gate extension 26 extends over a small portion of gate dielectric 24. See, for example, column 3, lines 11-67, column 4, lines 22-35, and Figure

1F of Mazure. In Mazure, gate dielectric 24 is thicker than gate dielectric 14. See, for example, column 3, lines 46-48 and Figure 1F of Mazure.

However, in Mazure, after gate dielectric 14 has been formed, gate dielectric 24 is formed over gate dielectric 14. See, for example, column 3, lines 46-48 and Figures 1B and 1C of Mazure. Thus, Mazure fails to teach, disclose, or suggest a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, as specified in amended independent claim 8. Furthermore, in Mazure, gate dielectric 24 is formed after gate 16 has been formed on gate dielectric 14. Thus, Mazure provides no motivation for using a single gate insulating layer having two different thicknesses, as specified in amended independent claim 8.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 8, is not taught, disclosed, or suggested by Mazure. Thus, amended independent claim 8 is patentably distinguishable over Mazure. As such, claim 17 depending from amended independent claim 8 is, *a fortiori*, also patentably distinguishable over Mazure for at least the reasons presented above and also for additional limitation contained in the dependent claim.

B. Rejection of Claims 9 and 22 under 35 USC §103(a)

The Examiner has rejected claims 9 and 22 under 35 USC §103(a) as being unpatentable over Mazure in view of U.S. patent number 6,429,072 to Masaru Tsukiji ("Tsukiji"). For the reasons discussed below, Applicants respectfully submits that the present invention, as defined by amended independent claim 9, is patentably distinguishable over Mazure and Tsukiji, singly or in combination.

The present invention, as defined by amended independent claim 9, includes, among other things, a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, and where the first thickness is greater than the second thickness. The present invention, as defined by amended independent claim 9, provides similar advantages as discussed above in relation to the present invention, as defined by amended independent claim 8.

In contrast, as discussed above, Mazure does not teach, disclose, or suggest a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, and where the first thickness is greater than the second thickness.

In contrast, Tsukiji does not teach, disclose, or suggest a single gate insulating layer situated over an entire length of a third region and substantially less than an entire length of each of a first region and a second region, where the single gate insulating layer has a first thickness situated over the first and second regions and a second thickness situated over the third region, and where the first thickness is greater than the second thickness. Tsukiji specifically discloses gate oxide film 102 situated on the top surface of the channel region of semiconductor substrate 101 and inter-layer insulators 122 situated on side walls and top surfaces of source side and drain side interconnections 104a and 105a, which overly respective source and drain regions 104 and 105. See, for example, column 8, lines 25-26, column 9, lines 12-19, and Figure 5E of Tsukiji. In Tsukiji, inter-layer insulators 122 are thicker than gate oxide film 102. See, for example, Tsukiji, column 8, lines 1-2.

In Tsukiji, the top surface of the channel region of semiconductor substrate 101 is defined between source and drain regions 104 and 105. See, for example, Tsukiji, column 7, lines 54-57. Thus, in Tsukiji, gate oxide film 102 is situated on the top surface of the channel region of semiconductor substrate 10 and situated between source and drain regions 104 and 105. Consequently, in Tsukiji, gate oxide film 102 is not situated over a portion of source and drain regions 104 and 105. Thus, Tsukiji fails to teach, disclose, or suggest a single gate insulating layer situated over an entire length of a third region, which is situated between first and second regions and which has an opposite conduction type than the first and second regions, and over substantially less than an

entire length of each of the first and second regions, as specified in amended independent claim 9. Thus, Tsukiji fails to cure the basic deficiencies of Mazure discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 9, is not taught, disclosed, or suggested by Mazure and Tsukiji, singly or in combination thereof. Thus, amended independent claim 9 is patentably distinguishable over Mazure and Tsukiji. As such, claim 12 depending from amended independent claim 9 is, *a fortiori*, also patentably distinguishable over Mazure and Tsukiji for at least the reasons presented above and also for additional limitation contained in the dependent claim.

C. Rejection of Claims 14-16 and 19-21 under 35 USC §103(a)

The Examiner has rejected claims 14-16 and 19-21 under 35 USC §103(a) as being unpatentable over Mazure in view of Tsukiji and U.S. patent number 6,432,762 B1 to Libera et al. As discussed above, amended independent claim 8 is patentably distinguishable over Mazure and amended independent claim 9 is patentably distinguishable over Mazure and Tsukiji. As such, claims 14-16 depending from amended independent claim 8 are, *a fortiori*, also patentably distinguishable over Mazure for at least the reasons presented above and also for the additional limitations contained in each dependent claim. Furthermore, claims 19-21 depending from amended independent claim 9 are, *a fortiori*, also patentably distinguishable over Mazure and Tsukiji for at least

the reasons presented above and also for the additional limitations contained in each dependent claim.

D. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 8 and 9, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 8, 9, 14-17, and 19-22 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 8, 9, 14-17, and 19-22 pending in the present application is respectfully requested.

Attorney Docket No.: 0180129

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